CLAIMS

What is claimed is:

1. A method for creating a cascaded chain of clocked half-rail differential logic circuits, said method comprising:

providing a first clocked half-rail differential logic circuit, said first clocked half-rail differential logic circuit comprising:

a first clocked half-rail differential logic circuit clock input terminal;

at least one first clocked half-rail differential logic circuit data input terminal; and

at least one first clocked half-rail differential logic circuit data output terminal;

providing a second clocked half-rail differential logic circuit, said second clocked half-rail differential logic circuit comprising:

a second clocked half-rail differential logic circuit clock input terminal;

at least one second clocked half-rail differential logic circuit data input terminal; and

at least one second clocked half-rail differential logic circuit data output terminal;

coupling a first clock signal to said first clocked half-rail differential logic circuit clock input terminal;

coupling a second clock signal to said second clocked half-rail differential logic circuit clock input terminal;

coupling said at least one first clocked half-rail differential logic circuit data output terminal to said at least one second clocked half-rail differential logic circuit data input terminal; and

delaying said second clock signal with respect to said first clock signal by a predetermined delay time.

2. The method of Claim 1 further comprising:

coupling a delay circuit between said first clocked half-rail differential logic circuit clock input terminal and said second clocked half-rail differential logic circuit clock input terminal for delaying said second clock signal with respect to said first clock signal by said predetermined delay time.

3. The method of Claim 2, wherein;

said delay circuit comprises at least one inverter.

4. The method of Claim 2, wherein;

said delay circuit comprises at least two inverters.

5. A method for creating a cascaded chain of clocked half-rail differential logic circuits, said method comprising:

providing a first supply voltage;

providing a second supply voltage;

providing a first clocked half-rail differential logic circuit, said first clocked half-rail differential logic circuit comprising:

a first clocked half-rail differential logic circuit out terminal;

a first clocked half-rail differential logic circuit out-not terminal;

a first transistor, said first transistor comprising a first transistor first flow electrode, a first transistor second flow electrode and a first transistor control electrode, said first supply voltage being coupled to said first transistor first flow electrode;

a second transistor, said second transistor comprising a second transistor first flow electrode, a second transistor second flow electrode and a second transistor control electrode, said first transistor second flow electrode being coupled to said second transistor first flow electrode, said second transistor second flow electrode being coupled to said first clocked half-rail differential logic circuit out terminal;

a third transistor, said third transistor comprising a third transistor first flow electrode, a third transistor second flow electrode and a third transistor control electrode, said first transistor second flow electrode being coupled to said third transistor first flow electrode, said third transistor second flow electrode being coupled to said first clocked half-rail differential logic circuit out-not terminal;

a fourth transistor, said fourth transistor comprising a fourth transistor first flow electrode, a fourth transistor second flow electrode and a fourth transistor control electrode, said second transistor control electrode being coupled to said fourth transistor first flow electrode and said first clocked half-rail differential logic circuit out-not terminal, said third transistor control electrode being

coupled to said fourth transistor second flow electrode and said first clocked half-rail differential logic circuit out terminal;

a logic block, said logic block comprising a logic block first input terminal, a logic block second input terminal, a logic block out terminal, a logic block out-not terminal and a logic block fifth terminal, said logic block out terminal being coupled to said first clocked half-rail differential logic circuit out terminal, said logic block out-not terminal being coupled to said first clocked half-rail differential logic circuit out-not terminal;

a fifth transistor, said fifth transistor comprising a fifth transistor first flow electrode, a fifth transistor second flow electrode and a fifth transistor control electrode, said fifth transistor first flow electrode being coupled to said logic block fifth terminal, said fifth transistor second flow electrode being coupled to said second supply voltage;

coupling a first clock signal to said fifth transistor control electrode of said fifth transistor of said first clocked half-rail differential logic circuit;

coupling a first clock-not signal to said first transistor control electrode of said first transistor of said first clocked half-rail differential logic circuit and said fourth transistor control electrode of said fourth transistor of said first clocked half-rail differential logic circuit;

providing a second clocked half-rail differential logic circuit, said second clocked half-rail differential logic circuit comprising:

a second clocked half-rail differential logic circuit out terminal;

a second clocked half-rail differential logic circuit out-not terminal;

a first transistor, said first transistor comprising a first transistor first flow electrode, a first transistor second flow electrode and a first transistor control electrode, said first supply voltage being coupled to said first transistor first flow electrode;

a second transistor, said second transistor comprising a second transistor first flow electrode, a second transistor second flow electrode and a second transistor control electrode, said first transistor second flow electrode being coupled to said second transistor first flow electrode, said second transistor second flow electrode being coupled to said second clocked half-rail differential logic circuit out terminal;

a third transistor, said third transistor comprising a third transistor first flow electrode, a third transistor second flow electrode and a third transistor control electrode, said first transistor second flow electrode being coupled to said third transistor first flow electrode, said third transistor second flow electrode being coupled to said second clocked half-rail differential logic circuit out-not terminal;

a fourth transistor, said fourth transistor comprising a fourth transistor first flow electrode, a fourth transistor second flow electrode and a fourth transistor control electrode, said second transistor control electrode being coupled to said fourth transistor first flow electrode and said second clocked half-rail differential logic circuit out-not terminal, said third transistor control electrode being

coupled to said fourth transistor second flow electrode and said second clocked half-rail differential logic circuit out terminal;

a logic block, said logic block comprising a logic block first input terminal, a logic block second input terminal, a logic block out terminal, a logic block out-not terminal and a logic block fifth terminal, said logic block first input terminal being coupled to said first clocked half-rail differential logic circuit out terminal, said logic block second input terminal being coupled to said first clocked half-rail differential logic circuit out-not terminal, said logic block out terminal being coupled to said second clocked half-rail differential logic circuit out terminal, said logic block out-not terminal being coupled to said second clocked half-rail differential logic circuit out-not terminal;

a fifth transistor, said fifth transistor comprising a fifth transistor first flow electrode, a fifth transistor second flow electrode and a fifth transistor control electrode, said fifth transistor first flow electrode being coupled to said logic block fifth terminal, said fifth transistor second flow electrode being coupled to said second supply voltage;

coupling a second clock signal to said fifth transistor control electrode of said fifth transistor of said second clocked half-rail differential logic circuit;

coupling a second clock-not signal to said first transistor control electrode of said first transistor of said second clocked half-rail differential logic circuit and said fourth transistor control electrode of said fourth transistor of said second clocked half-rail differential logic circuit;

delaying said second clock signal with respect to said first clock signal by a predetermined delay time; and

delaying said second clock-not signal with respect to said first clock-not signal by said predetermined delay time.

6. The method of Claim 5, further comprising:

providing a delay circuit;

coupling said delay circuit between said fifth transistor control electrode of said fifth transistor of said first clocked half-rail differential logic circuit and said fifth transistor control electrode of said fifth transistor of said second clocked half-rail differential logic circuit;

coupling said delay circuit between said first transistor control electrode of said first transistor of said first clocked half-rail differential logic circuit and said first transistor control electrode of said first transistor of said second clocked half-rail differential logic circuit;

coupling said delay circuit between said fourth transistor control electrode of said fourth transistor of said first clocked half-rail differential logic circuit and said fourth transistor control electrode of said fourth transistor of said second clocked half-rail differential logic circuit;

said delay circuit thereby providing said predetermined delay time.

7. The method of Claim 6, wherein;

said delay circuit comprises at least one inverter.

8. The method of Claim 6, wherein;
said delay circuit comprises at least two inverters.

9. The method of Claim 1, wherein;
said logic block of said first clocked half-rail differential logic circuit and said logic block of said second clocked half-rail differential logic circuit comprise differential logic.

10. The method of Claim 1, wherein;
said logic block of said first clocked half-rail differential logic circuit and said logic block of said second clocked half-rail differential logic circuit comprise differential logic gates.

11. The method of Claim 1, wherein;
said logic block of said first clocked half-rail differential logic circuit and said logic block of said second clocked half-rail differential logic circuit comprise inverters.

12. The method of Claim 1, wherein;
said first supply voltage is Vdd and said second supply voltage is ground.

13. The method of Claim 12, wherein;
said first transistor, said second transistor and said third transistor of said first clocked half-rail differential logic circuit and said first transistor, said second transistor and said third transistor of

said second clocked half-rail differential logic circuit are PFETs.

14. The method of Claim 13, wherein;

said fourth transistor and said fifth transistor of said first clocked half-rail differential logic circuit and said fourth transistor and said fifth transistor of said second clocked half-rail differential logic circuit are NFETs.

15. A method for creating a clocked half-rail differential logic circuit, said method comprising:

providing a first supply voltage;

providing a second supply voltage;

providing a clocked half-rail differential logic circuit out terminal;

providing a clocked half-rail differential logic circuit out-not terminal;

providing a first transistor, said first transistor comprising a first transistor first flow electrode, a first transistor second flow electrode and a first transistor control electrode,

coupling said first supply voltage to said first transistor first flow electrode;

providing a second transistor, said second transistor comprising a second transistor first flow electrode, a second transistor second flow electrode and a second transistor control electrode;

coupling said first transistor second flow electrode to said second transistor first flow electrode;

coupling said second transistor second flow electrode to said clocked half-rail differential logic circuit out terminal;

providing a third transistor, said third transistor comprising a third transistor first flow electrode, a third transistor second flow electrode and a third transistor control electrode;

coupling said first transistor second flow electrode to said third transistor first flow electrode;

coupling said third transistor second flow electrode to said clocked half-rail differential logic circuit out-not terminal;

providing a fourth transistor, said fourth transistor comprising a fourth transistor first flow electrode, a fourth transistor second flow electrode and a fourth transistor control electrode;

coupling said second transistor control electrode to said fourth transistor first flow electrode and said clocked half-rail differential logic circuit out-not terminal;

coupling said third transistor control electrode to said fourth transistor second flow electrode and said clocked half-rail differential logic circuit out terminal;

providing a logic block, said logic block comprising a logic block first input terminal, a logic block second input terminal, a logic block out terminal, a logic block out-not terminal and a logic block fifth terminal;

coupling said logic block out terminal to said clocked half-rail differential logic circuit out terminal;

coupling said logic block out-not terminal to said clocked half-rail differential logic circuit out-not terminal;

providing a fifth transistor, said fifth transistor comprising a fifth transistor first flow electrode, a fifth transistor second flow electrode and a fifth transistor control electrode;

coupling said fifth transistor first flow electrode to said logic block fifth terminal;

coupling said fifth transistor second flow electrode to a second supply voltage;

providing a clock signal;

coupling said clock signal to said fifth transistor control electrode of said fifth transistor of said clocked half-rail differential logic circuit;

providing a clock-not signal; and

coupling said clock-not signal to said first transistor control electrode of said first transistor of said clocked half-rail differential logic circuit and said fourth transistor control electrode of said fourth transistor of said clocked half-rail differential logic circuit.

16. The method of Claim 15, wherein;

said logic block of said clocked half-rail differential logic circuit comprises differential logic.

17. The method of Claim 15, wherein;

said logic block of said clocked half-rail differential logic circuit comprises differential logic gates.

18. The method of Claim 15, wherein;

said logic block of said clocked half-rail differential logic circuit comprises an inverter.

19. The method of Claim 15, wherein;

said first supply voltage is Vdd and said second supply voltage is ground.

20. The method of Claim 19, wherein;
said first transistor, said second transistor and said third transistor are PFETs.

21. The method of Claim 20, wherein;
said fourth transistor and said fifth transistor are NFETs.